library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity bcdcount is

 Port ( clr,updn : in std\_logic;

 clk : in std\_logic;

 pre : in std\_logic;

 x : out std\_logic\_vector(3 downto 0));

end bcdcount;

architecture Behavioral of bcdcount is

signal y: std\_logic\_vector(3 downto 0);

signal divider: std\_logic\_vector(21 downto 0);

signal sclk:std\_logic;

begin

process(clk)

begin

if (clk'event and clk='1') then divider<=divider+1;

end if;

end process;

sclk<=divider(21);

process(clr, pre, sclk)

begin

 if (clr='0') then y<="0000";

 else if (pre='0') then y<="1001";

 else if (sclk'event and sclk = '1') then

 if (updn = '1') then y<=y+1;

 if(y = "1001") then y<="0000";

 end if;

 else y<=y-1;

 if (y = "0000") then y<="1001";

 end if;

 end if; end if;

 end if; end if;

end process;

x<=y;

end behavioral;