-------------------------------------**BINARY TO GRAY**---------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity BINTOGRAY is

 Port ( D : in STD\_LOGIC\_VECTOR (03 downto 0);

 Y : out STD\_LOGIC\_VECTOR (03 downto 0));

end BINTOGRAY;

architecture DATAFLOW of BINTOGRAY is

begin

y(3) <= d(3);

 y(2) <= d(3) xor d(2);

 y(1) <= d(2) xor d(1);

 y(0) <= d(1) xor d(0);

end DATAFLOW;



-------------------------------------**GRAY TO BINARY**---------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity GRAYTOBIN is

 Port ( D : in STD\_LOGIC\_VECTOR (03 downto 0);

 Y : out STD\_LOGIC\_VECTOR (03 downto 0));

end GRAYTOBIN;

architecture Behavioral of GRAYTOBIN is

begin

PROCESS (D)

 variable TEMP : STD\_LOGIC\_VECTOR(3 DOWNTO 0);

 BEGIN

 TEMP(3) := D(3);

 TEMP(2) := (D(2) XOR TEMP(3));

 TEMP(1) := (D(1) XOR TEMP(2));

 TEMP(0) := (D(0) XOR TEMP(1));

 y <= TEMP;

 END PROCESS;

end Behavioral;

-------------------------------------**GRAY TO BINARY**---------------------------------------------



-------------------------------------**MUX 4:1 USING EXPRESSION**---------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity MUX41EXPR is

 Port ( D : in STD\_LOGIC\_VECTOR (03 downto 0);

 S1 : in STD\_LOGIC;

 S0 : in STD\_LOGIC;

 Y : out STD\_LOGIC);

end MUX41EXPR;

architecture DATAFLOW of MUX41EXPR is

begin

Y <= ((NOT S1) AND (NOT S0) AND D(0)) OR ((NOT S1) AND S0 AND D(1)) OR (S1 AND (NOT S0) AND D(2)) OR (S1 AND S0 AND D(3));

end DATAFLOW;



-------------------------------------**MUX 4:1 USING CASE**---------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity MUX41CASE is

 Port ( SEL : in STD\_LOGIC\_VECTOR (01 downto 0);

 D : in STD\_LOGIC\_VECTOR (03 downto 0);

 Y : out STD\_LOGIC);

end MUX41CASE;

architecture Behavioral of MUX41CASE is

begin

PROCESS (D,SEL)

BEGIN

 CASE SEL IS

 WHEN "00" => Y <= D(0);

 WHEN "01" => Y <= D(1);

 WHEN "10" => Y <= D(2);

 WHEN "11" => Y <= D(3);

 WHEN OTHERS => Y <= 'Z';

 END CASE;

END PROCESS;

end Behavioral;

-------------------------------------**MUX 4:1 USING CASE**---------------------------------------------

