**EXPERIMENT NO. 8**

**Program :**

module jkff(j,k,clk,q);

output q;

input j,k,clk;

reg q;

always @(posedge clk)

case({j,k})

2'b00:q=q;

2'b01:q=1'b0;

2'b10:q=1'b1;

2'b11:q=~q;

endcase

endmodule

**Test Bench :**

`timescale 1ns/1ps

module jktest\_v;

reg j,k,clk;

wire q;

jkff jk1(j,k,clk,q);

initial

clk=0;

always

#50 clk=~clk;

initial

begin

{j,k}=2'b00;

#50 {j,k}=2'b00;

#50 {j,k}=2'b01;

#50 {j,k}=2'b10;

#50 {j,k}=2'b11;

end

endmodule

RTL SCHEMATIC :



TECHNOLOGY SCHEMATIC : 

Output :



=========================================================================

\* Final Report \*

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Final Results

RTL Top Level Output File Name : jkff.ngr

Top Level Output File Name : jkff

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : YES

Target Technology : Automotive 9500XL

Macro Preserve : YES

XOR Preserve : YES

Clock Enable : YES

wysiwyg : NO

Design Statistics

# IOs : 4

Cell Usage :

# BELS : 8

# AND2 : 2

# INV : 4

# OR2 : 1

# OR3 : 1

# FlipFlops/Latches : 1

# FD : 1

# IO Buffers : 4

# IBUF : 3

# OBUF : 1

=========================================================================

CPU : 1.45 / 1.64 s | Elapsed : 1.00 / 2.00 s

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Total memory usage is 130424 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)