**4 : 1 Multiplexer**

**Program:**

module mux4to1(y,i0,i1,i2,i3,s0,s1);

input i0,i1,i2,i3,s0,s1;

output y;

wire y0,y1,y2,y3,s01,s11;

not (s11,s1);

not(s01,s0);

and (y0,i0,s01,s11);

and (y1,i1,s0,s11);

and (y2,i2,s01,s1);

and (y3,i3,s0,s1);

or (y,y0,y1,y2,y3);

endmodule

**Testbench:**

`timescale 1ns/1ps

module muxtest\_v;

reg a,b,c,d,s1,s0;

wire z;

mux4to1 m1(z,a,b,c,d,s1,s0);

initial

begin

a=0; b=1; c=1; d=0; s1=0; s0=0;

#50 s1=0; s0=1;

#50 s1=1; s0=0;

#50 s1=1; s0=1;

#50;

end

endmodule

**Wave form:**



**RTL Schematic:**



**Technology Schematic:**



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\* Final Report \*

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Final Results

RTL Top Level Output File Name : mux4to1.ngr

Top Level Output File Name : mux4to1

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : YES

Target Technology : CoolRunner XPLA3 CPLDs

Macro Preserve : YES

XOR Preserve : YES

Clock Enable : YES

wysiwyg : NO

Design Statistics

# IOs : 7

Cell Usage :

# BELS : 12

# AND2 : 6

# INV : 3

# OR2 : 3

# IO Buffers : 7

# IBUF : 6

# OBUF : 1

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CPU : 1.51 / 1.70 s | Elapsed : 2.00 / 2.00 s

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Total memory usage is 115608 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)